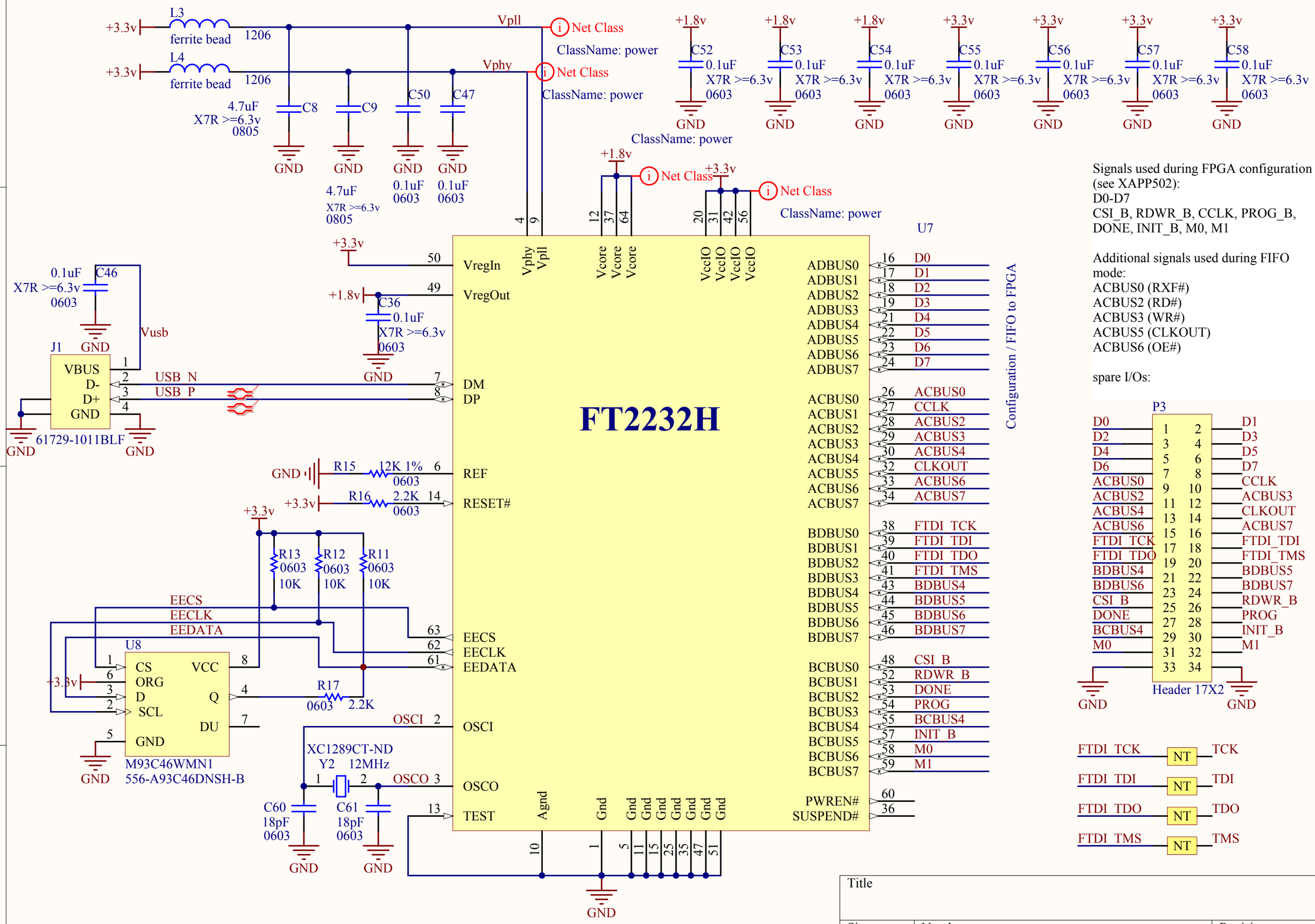
Inspired by http://www.ftdichip.com/Documents/DataSheets/DS_FT2232H_V206.pdf page 47



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Date: 7/6/2013		Sheet of
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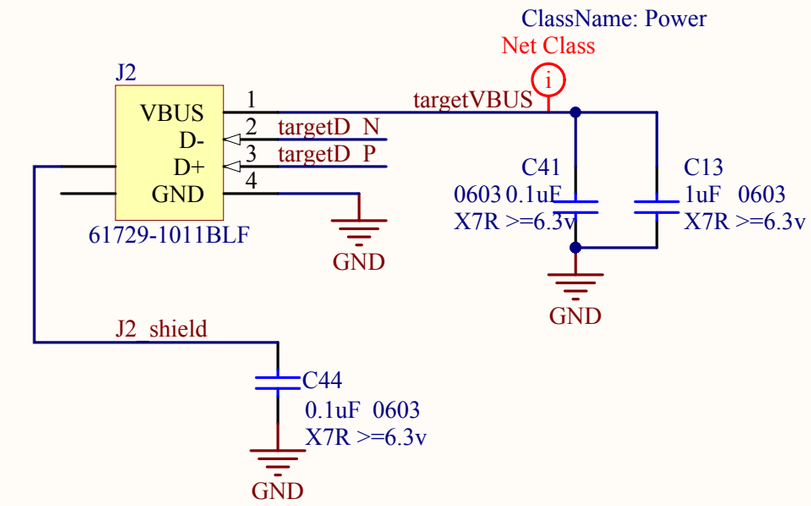

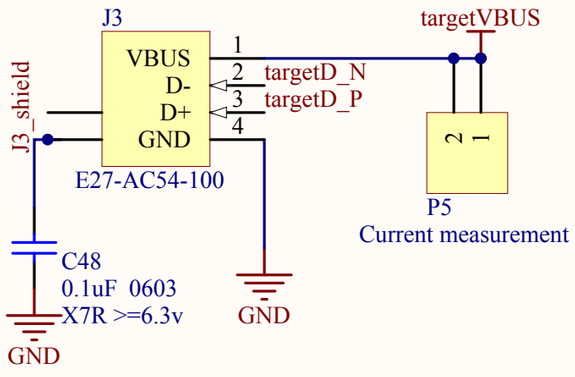

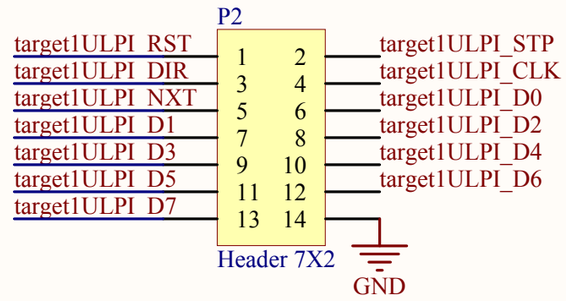

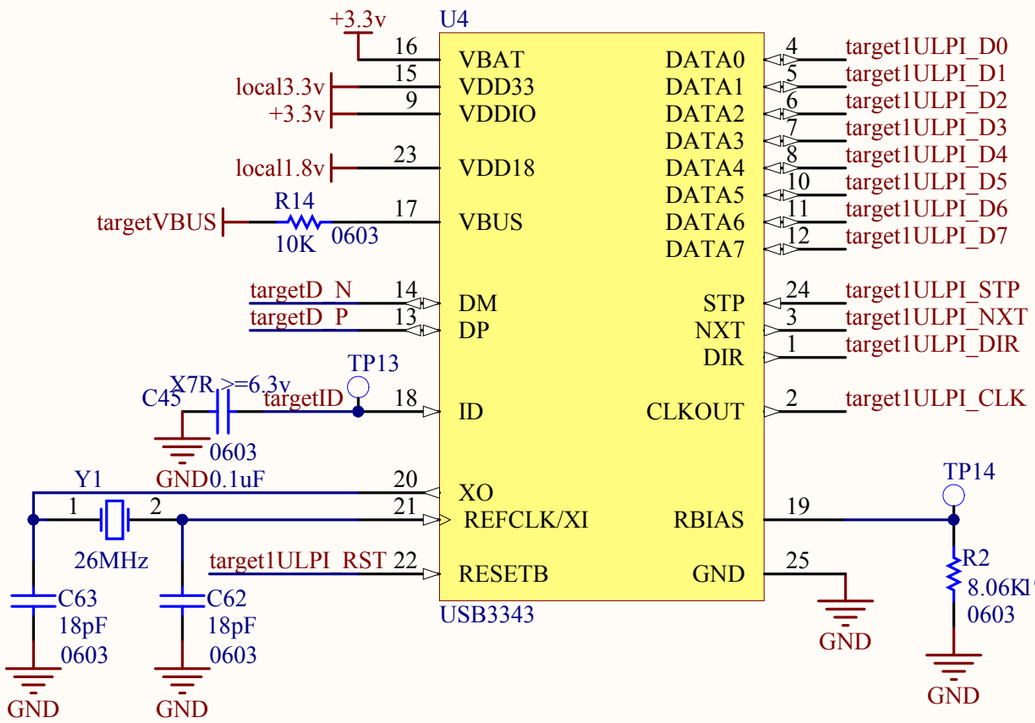

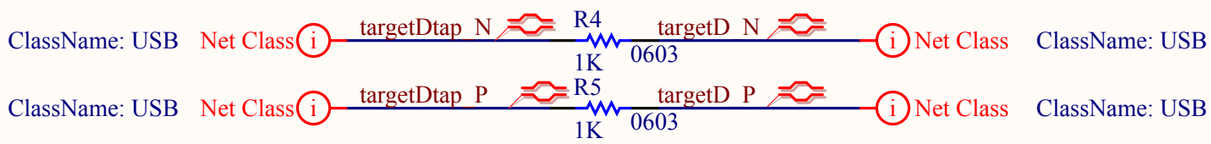

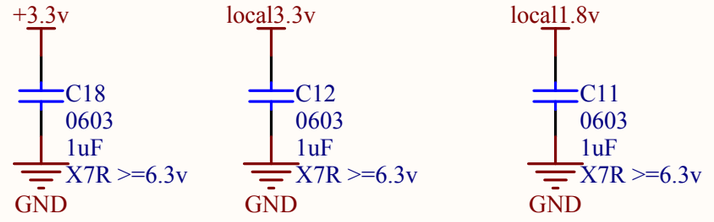

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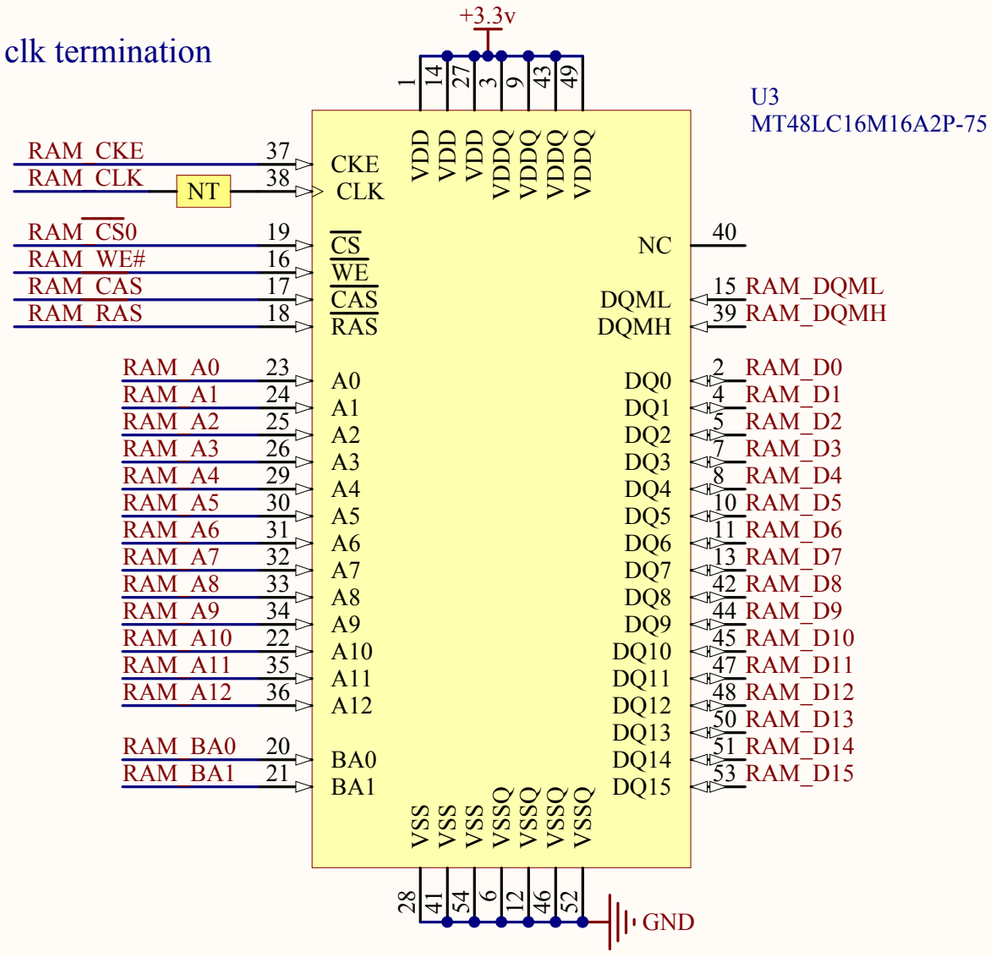
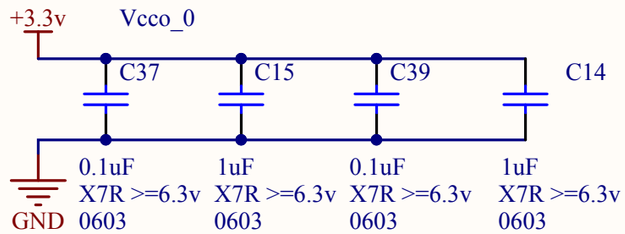
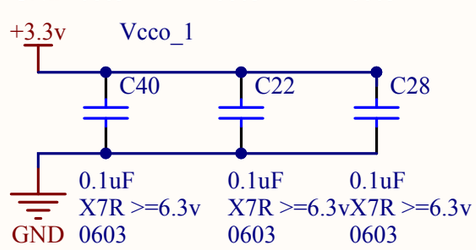
Date: 7/6/2013		Sheet 3 of
File: X:\ov\..\target USB interfaces v3.SchDoc		Drawn By:

optional RAM clk termination







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Date: 7/6/2013		Sheet of
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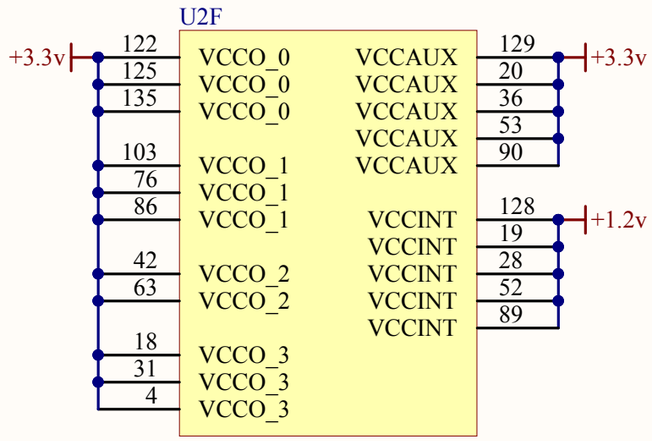
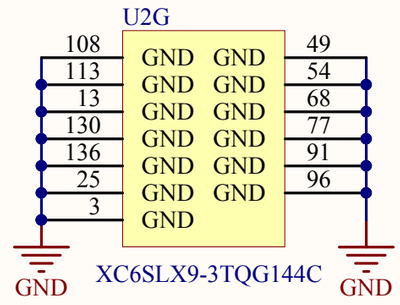
MHole3.2mm

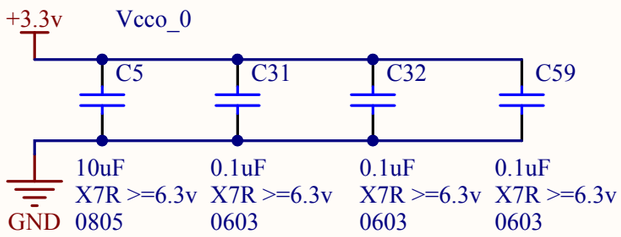
MHole3.2mm

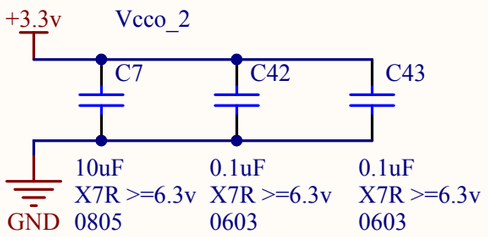
MHole3.2mm

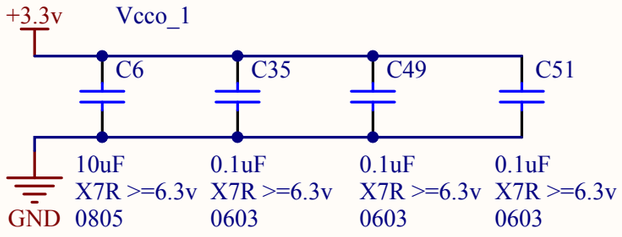
MHole3.2mm

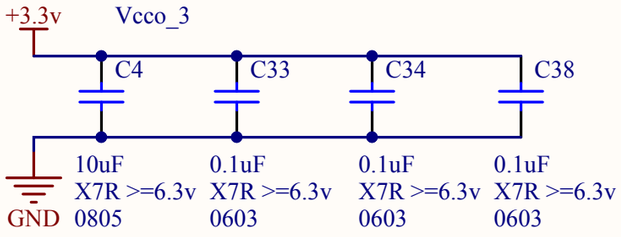


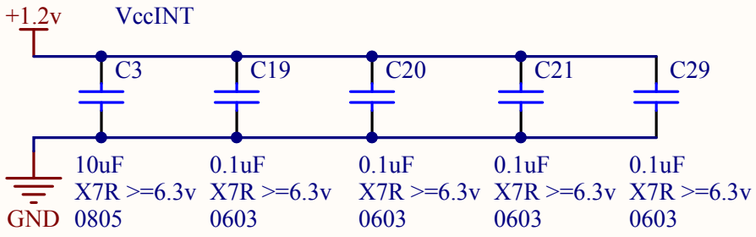


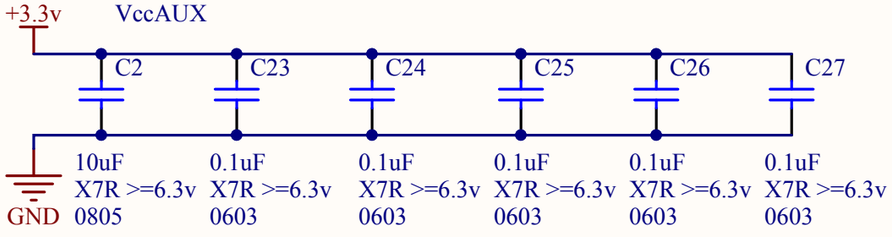












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Size: A	Number	Revision
Date: 7/6/2013		Sheet 13 of
File: X:\ov\..\FPGA power v3.SchDoc		Drawn By:

U2C

BANK 2

IO_L1P_CCLK_2 70 CCLK
IO_L1N_M0_CMPMISO_2 69 M0
IO_L2P_CMPCLK_2 67 SW1
IO_L2N_CMPMOSI_2 66 TP15
IO_L3P_D0_DIN_MISO_MISO1_2 65 D0
IO_L3N_MOSI_CSI_B_MISO0_2 64 CSI_B
IO_L12P_D1_MISO2_2 62 D1
IO_L12N_D2_MISO3_2 61 D2
IO_L13P_M1_2 60 M1
IO_L13N_D10_2 59 LED2
IO_L14P_D11_2 58 LED1
IO_L14N_D12_2 57 LED0
IO_L30P_GCLK1_D13_2 56 RAM_CKE
IO_L30N_GCLK0_USERCCLK_2 55 ACBUS0
IO_L31P_GCLK31_D14_2 51 CLKOUT
IO_L31N_GCLK30_D15_2 50
IO_L48P_D7_2 48 D7
IO_L48N_RDWR_B_VREF_2 47 RDWR_B
IO_L49P_D3_2 46 D3
IO_L49N_D4_2 45 D4
IO_L62P_D5_2 44 D5
IO_L62N_D6_2 43 D6
IO_L64P_D8_2 41 ACBUS2
IO_L64N_D9_2 40 ACBUS3
IO_L65P_INIT_B_2 39 INIT_B
IO_L65N_CSO_B_2 38 ACBUS6

XC6SLX9-3TQG144C

R3 1K 0603 OSCO

Signals used during FPGA configuration (see XAPP502):
D0-D7
CSI_B, RDWR_B, CCLK, PROG_B, DONE, INIT_B, M0, M1

Additional signals used during FIFO mode:
ACBUS0 (RXF#)
ACBUS2 (RD#)
ACBUS3 (WR#)
ACBUS5 (CLKOUT)
ACBUS6 (OE#)

spare I/Os:

U2D

BANK 3

IO_L1P_3 35 RAM_A4
IO_L1N_VREF_3 34 RAM_A5
IO_L2P_3 33 RAM_A6
IO_L2N_3 32 RAM_A7
IO_L36P_3 30 RAM_A8
IO_L36N_3 29 RAM_A9
IO_L37P_3 27 RAM_A11
IO_L37N_3 26 RAM_A12
IO_L41P_GCLK27_3 24 RAM_CLK
IO_L41N_GCLK26_3 23 RAM_DQMH
IO_L42P_GCLK25_TRDY2_3 22 RAM_D8
IO_L42N_GCLK24_3 21 RAM_D9
IO_L43P_GCLK23_3 17 RAM_D10
IO_L43N_GCLK22_IRDY2_3 16 RAM_D11
IO_L44P_GCLK21_3 15 RAM_D12
IO_L44N_GCLK20_3 14 RAM_D13
IO_L49P_3 12 RAM_D14
IO_L49N_3 11 RAM_D15
IO_L50P_3 10 RAM_A3
IO_L50N_3 9 RAM_A2
IO_L51P_3 8 RAM_A1
IO_L51N_3 7 RAM_A0
IO_L52P_3 6 RAM_A10
IO_L52N_3 5 RAM_BA1
IO_L83P_3 2 RAM_BA0
IO_L83N_VREF_3 1 RAM_CS0

XC6SLX9-3TQG144C

+3.3v
R6 330 0603 LED0 red 0603 LD1
R7 330 0603 LED1 red 0603 LD2
R8 330 0603 LED2 red 0603 LD3
R9 330 0603 GND green 0603 LD4

+3.3v
R1 0603 10
U5 VCC OUT EN GND 50MHz
C30 0.1uF X7R >=6.3v 0603
GND

Spare 50MHz clock for bringup

U2A

BANK 0

IO_L1P_HSWAPEN_0 144 RAM_RAS
IO_L1N_VREF_0 143 RAM_CAS
IO_L2P_0 142 RAM_WE#
IO_L2N_0 141 RAM_DQML
IO_L3P_0 140 RAM_D7
IO_L3N_0 139 RAM_D6
IO_L4P_0 138 RAM_D5
IO_L4N_0 137 RAM_D4
IO_L34P_GCLK19_0 134 RAM_D3
IO_L34N_GCLK18_0 133 RAM_D2
IO_L35P_GCLK17_0 132 RAM_D1
IO_L35N_GCLK16_0 131 RAM_D0
IO_L36P_GCLK15_0 127 TARGET1ULPI_RST
IO_L36N_GCLK14_0 126 TARGET1ULPI_STP
IO_L37P_GCLK13_0 124 TARGET1ULPI_DIR
IO_L37N_GCLK12_0 123 TARGET1ULPI_CLK
IO_L62P_0 121 TARGET1ULPI_NXT
IO_L62N_VREF_0 120 TARGET1ULPI_D0
IO_L63P_SCP7_0 119 TARGET1ULPI_D1
IO_L63N_SCP6_0 118 TARGET1ULPI_D2
IO_L64P_SCP5_0 117 TARGET1ULPI_D3
IO_L64N_SCP4_0 116 TARGET1ULPI_D4
IO_L65P_SCP3_0 115 TARGET1ULPI_D5
IO_L65N_SCP2_0 114 TARGET1ULPI_D6
IO_L66P_SCP1_0 112 TARGET1ULPI_D7
IO_L66N_SCP0_0 111 TP16

XC6SLX9-3TQG144C

U2B

BANK 1

IO_L1P_1 105 targetDtap_P
IO_L1N_VREF_1 104 targetDtap_N
IO_L32P_1 102 SPARE2
IO_L32N_1 101 SPARE3
IO_L33P_1 100 SPARE4
IO_L33N_1 99 SPARE5
IO_L34P_1 98 SPARE6
IO_L34N_1 97 SPARE7
IO_L40P_GCLK11_1 95 SPARE8
IO_L40N_GCLK10_1 94 SPARE9
IO_L41P_GCLK9_IRDY1_1 93 SPARE10
IO_L41N_GCLK8_1 92 SPARE11
IO_L42P_GCLK7_1 88 SPARE12
IO_L42N_GCLK6_TRDY1_1 87 SPARE13
IO_L43P_GCLK5_1 85 SPARE14
IO_L43N_GCLK4_1 84 SPARE15
IO_L45P_1 83 SPARE16
IO_L45N_1 82 SPARE17
IO_L46P_1 81 SPARE18
IO_L46N_1 80 SPARE19
IO_L47P_1 79 SPARE20
IO_L47N_1 78 SPARE21
IO_L74P_AWAKE_1 75 SPARE22
IO_L74N_DOUT_BUSY_1 74 SPARE23

XC6SLX9-3TQG144C

+3.3v P4 +3.3v

	1	2	
	3	4	
SPARE2	5	6	SPARE3
SPARE4	7	8	SPARE5
SPARE6	9	10	SPARE7
SPARE8	11	12	SPARE9
SPARE10	13	14	SPARE11
SPARE12	15	16	SPARE13
SPARE14	17	18	SPARE15
SPARE16	19	20	SPARE17
SPARE18	21	22	SPARE19
SPARE20	23	24	SPARE21
SPARE22	25	26	SPARE23
	27	28	

GND Header 14X2 GND

P1 +3.3v
1 GND
2
3 TCK
4
5 TDO
6 TDI
7
8 TMS
9
Header 9

DONE 71 DONE_2
PROG 37 PROGRAM_B_2
GND 73 SUSPEND
TDI 109 TCK
TDO 110 TDI
TCK 106 TDO
TMS 107 TMS
TP17 72 CMPCS_B_2

U2E

XC6SLX9-3TQG144C

+3.3v R10 10K 0603 SW1 1 2 4 3 GND GND SW1 TL1105LF160Q

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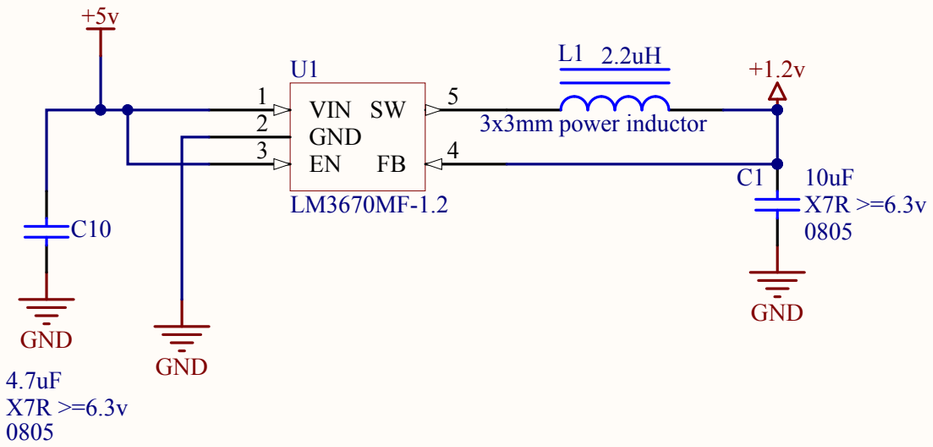
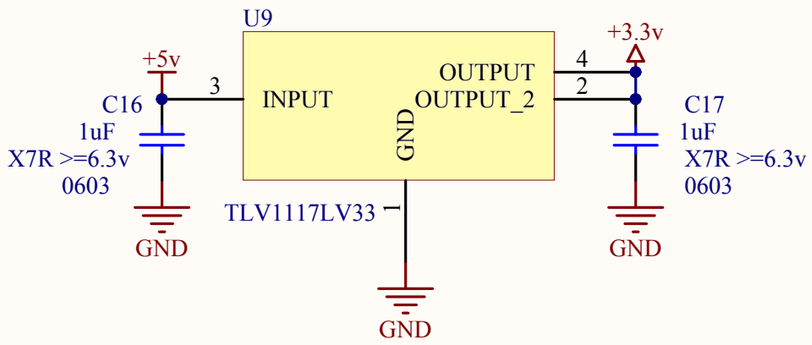
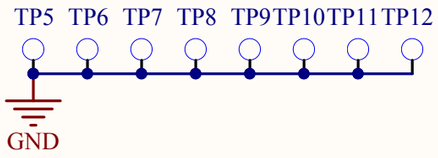
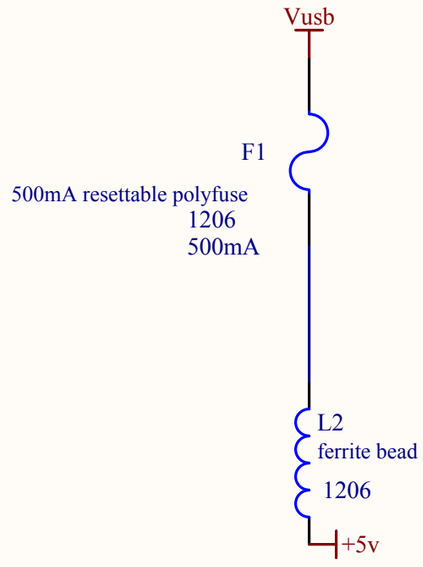
Size A	Number	Revision
Date: 7/6/2013		Sheet of
File: X:\ov\ov_ftdi\hardware\fpga.SchDoc		Drawn By:



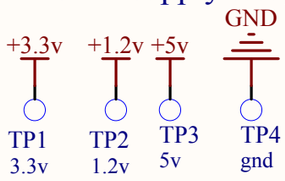


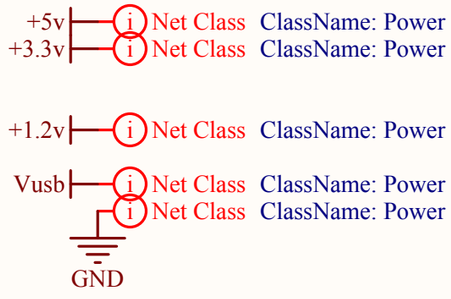
Ground clip pads





Power supply test points, top side





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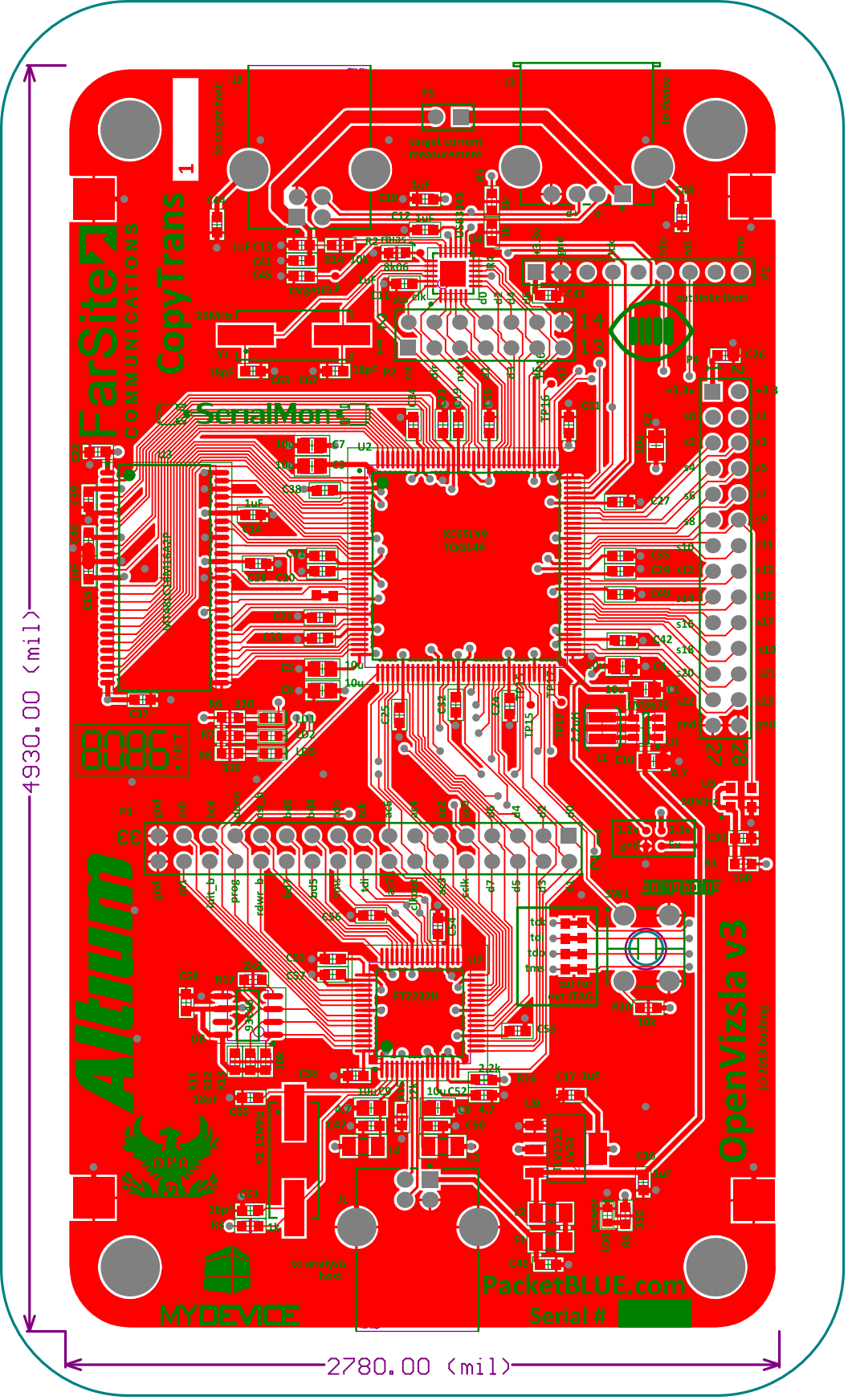

Top Layer

Top Overlay

Mechanical 1
Mech2 (Acrylic)
Mechanical 5

Multilayer

Mechanical 11
Mechanical 13
Mechanical 14
Mechanical 15
Mechanical 16

Size legend:
1 sq in

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SerialMon

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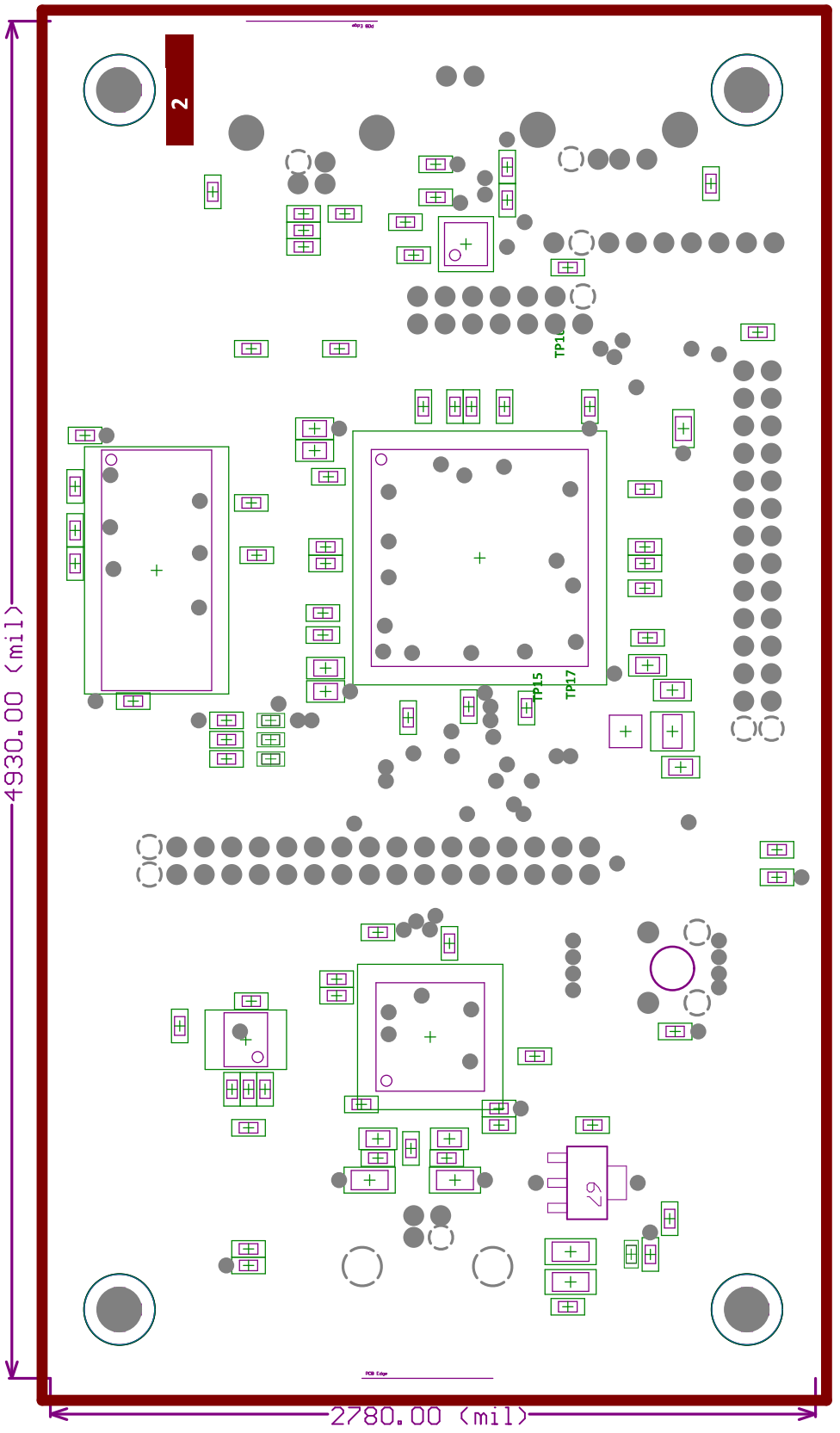


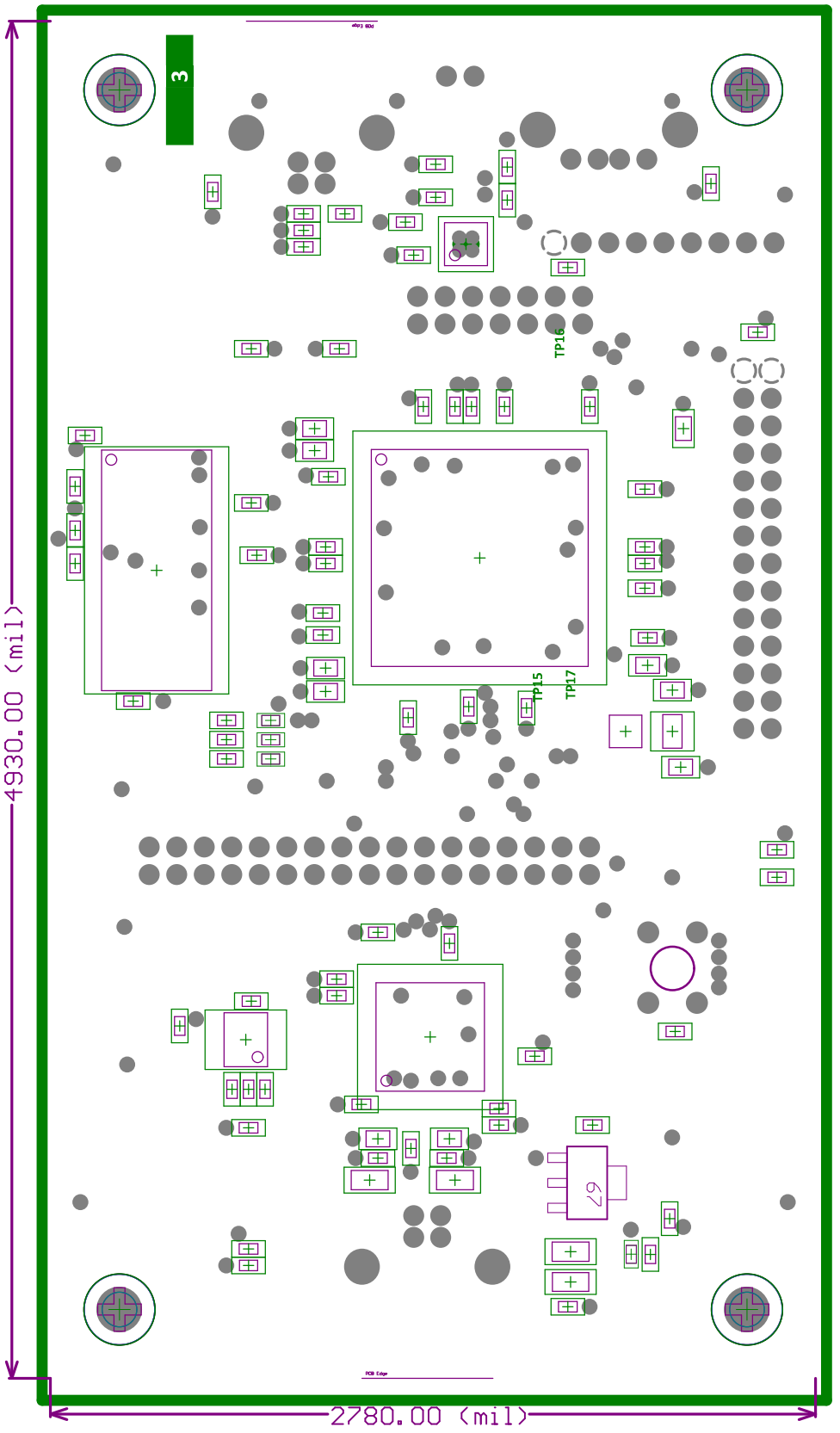
Layer 2 (Ground)

Mechanical 1

Mechanical 5

Multilayer

Mechanical 11
Mechanical 13
Mechanical 14
Mechanical 15
Mechanical 16

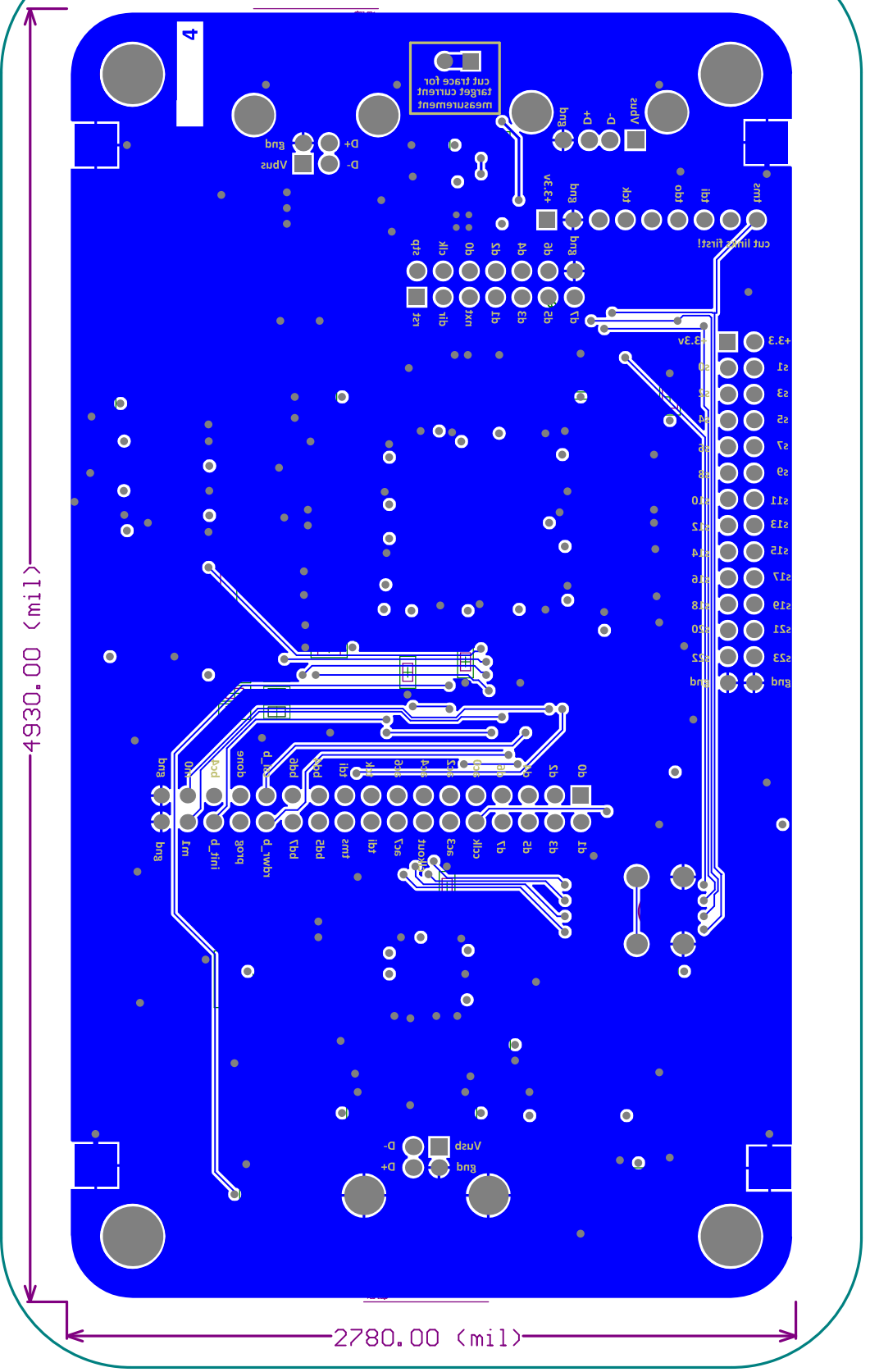


Layer3 (3.3v)
Mechanical 1

Mechanical 5

Mechanical 11
Mechanical 13
Mechanical 14
Mechanical 15
Mechanical 16

Multilayer



BottomLayer

Bottom Overlay

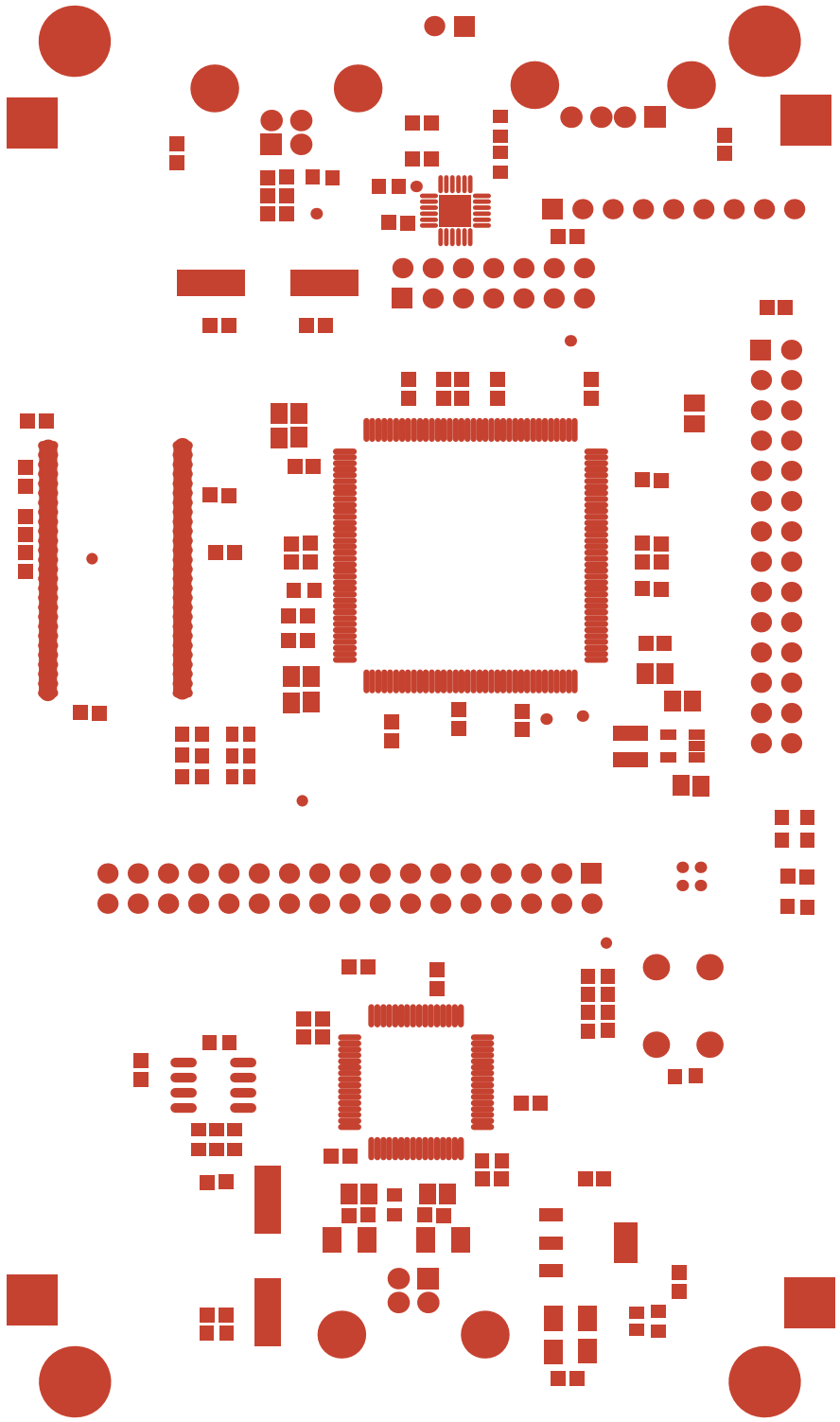
Mechanical 1
Mech2 (Acrylic)
Mechanical 5

Multilayer

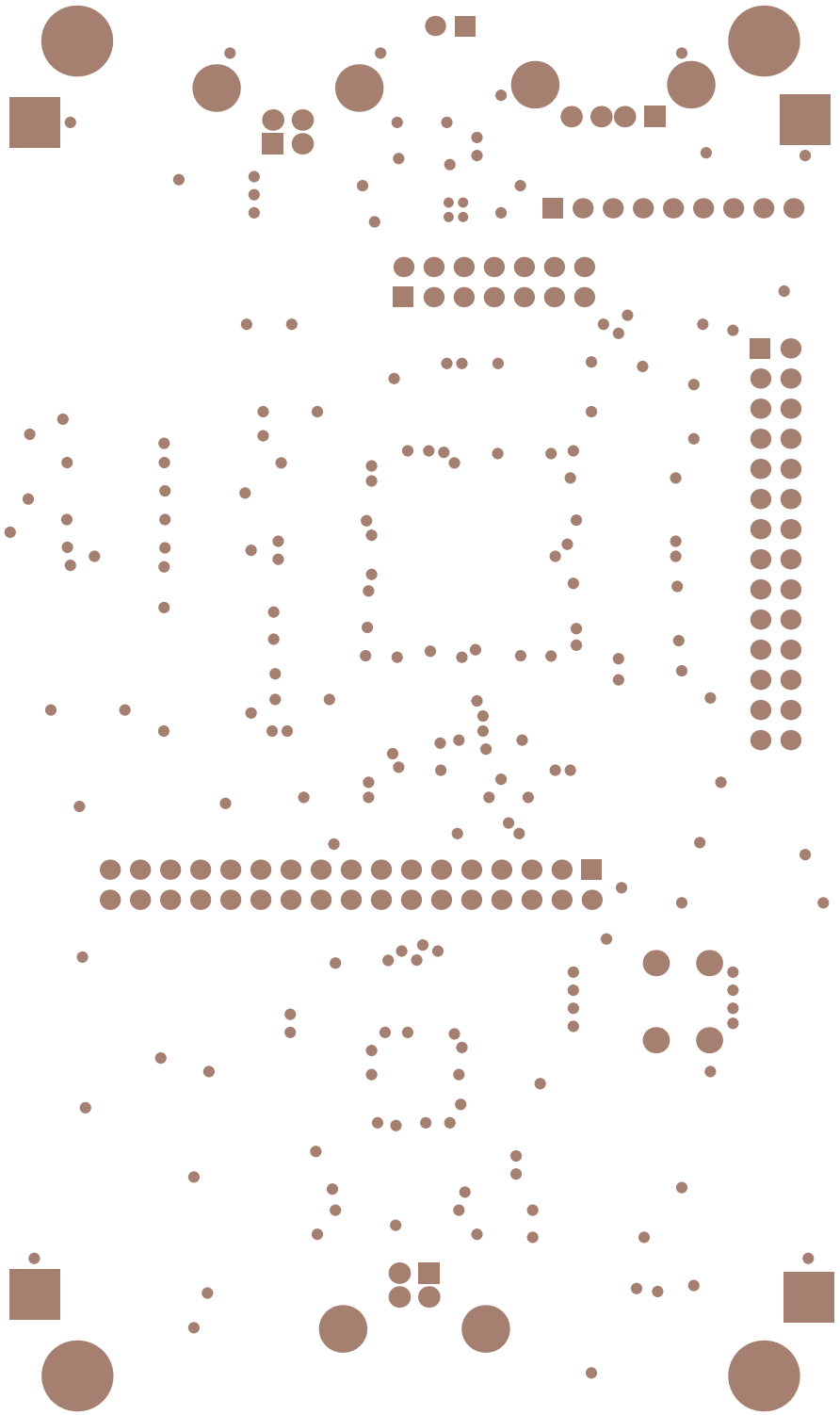
Mechanical 11
Mechanical 13
Mechanical 14
Mechanical 15
Mechanical 16

Size legend:
1 sq in

Top Solder



Bottom Solder



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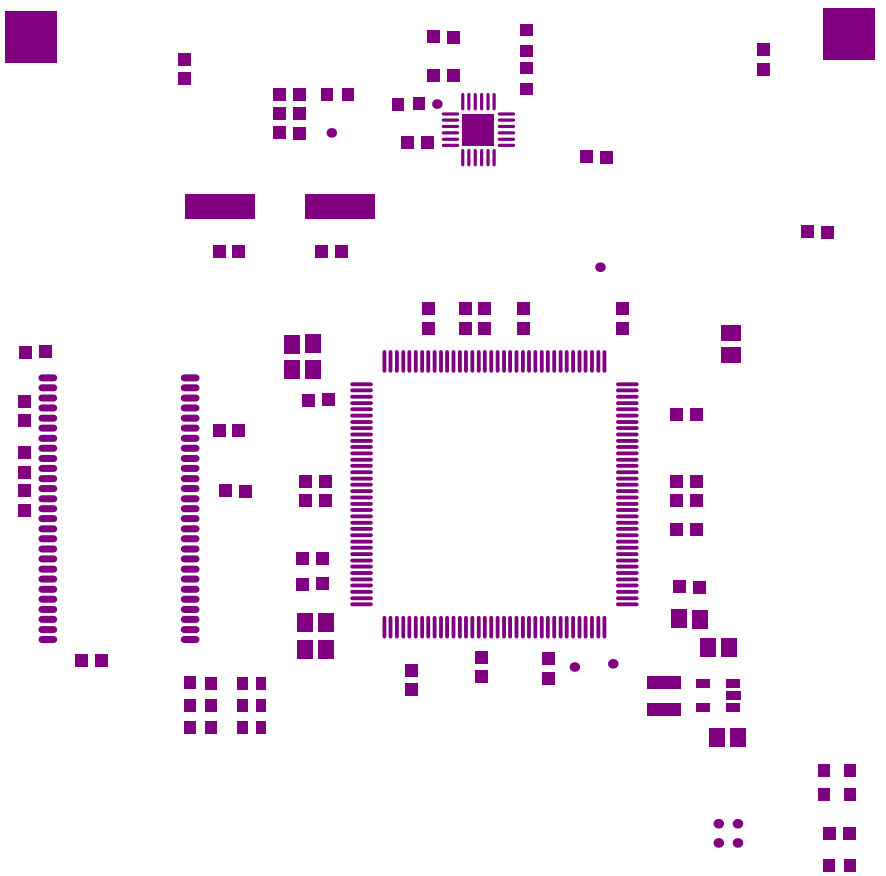
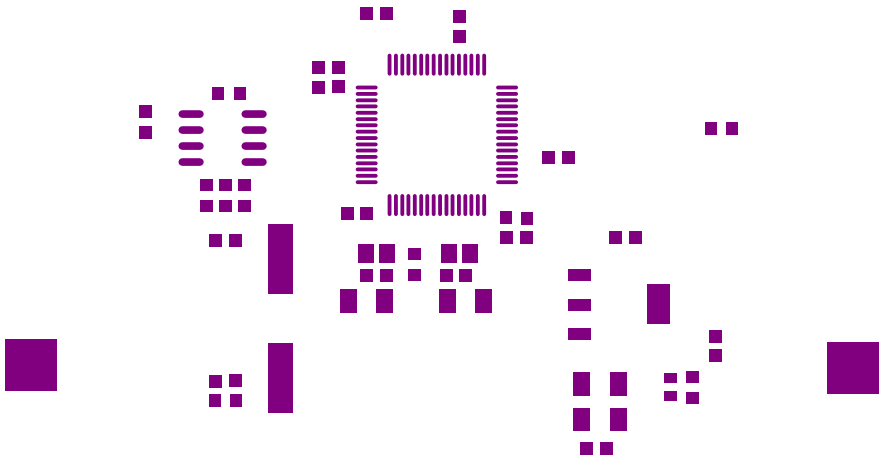
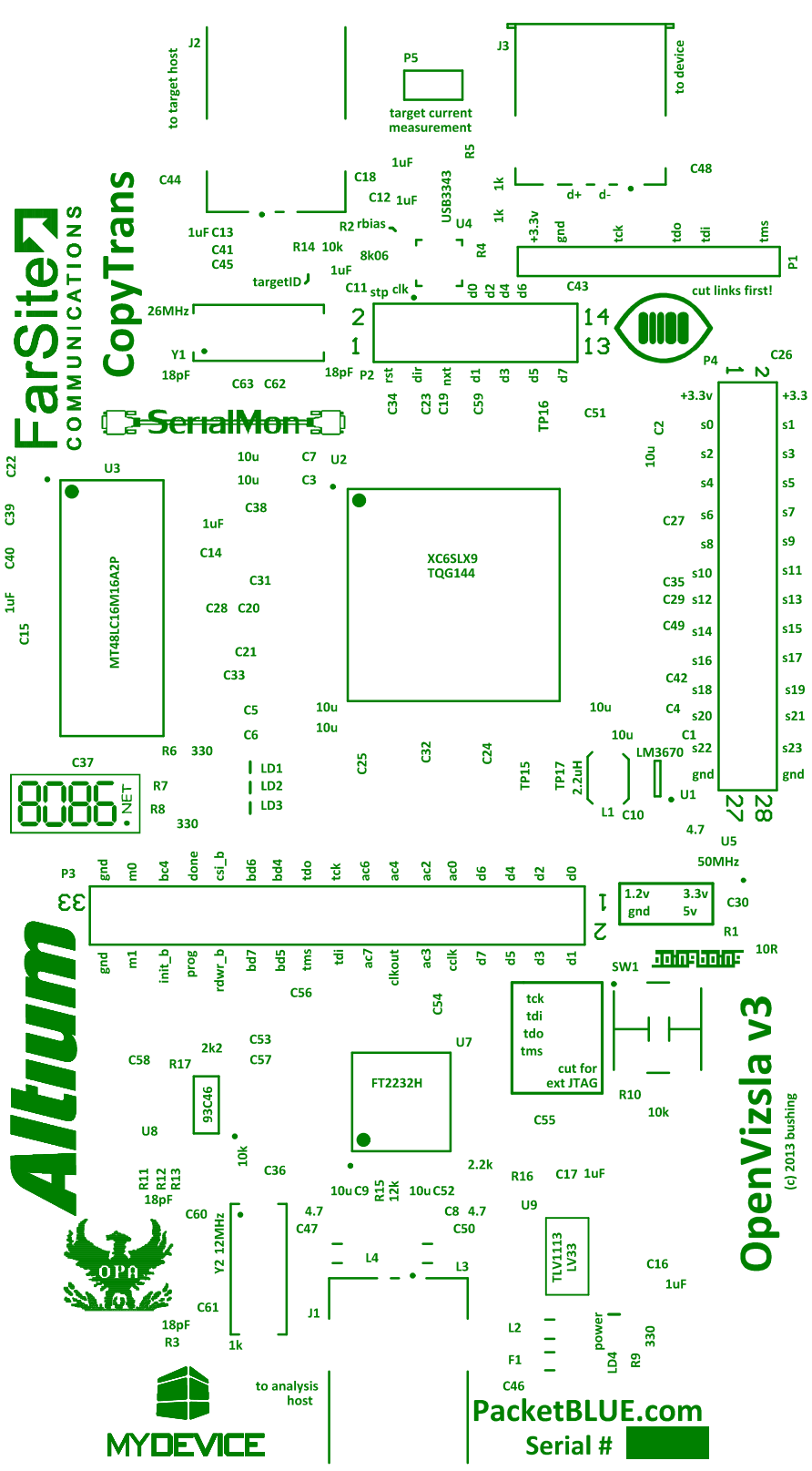




Top Overlay



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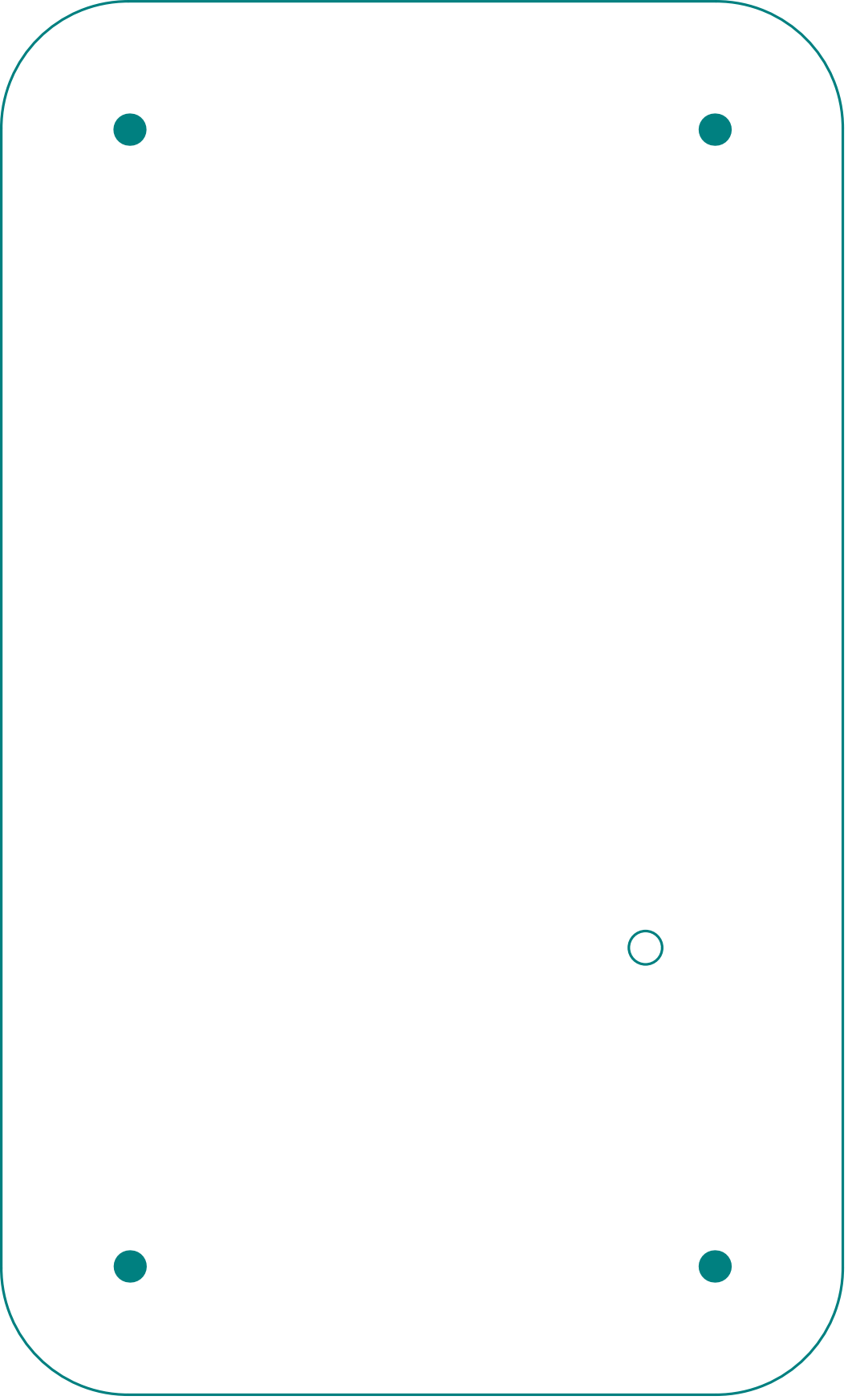
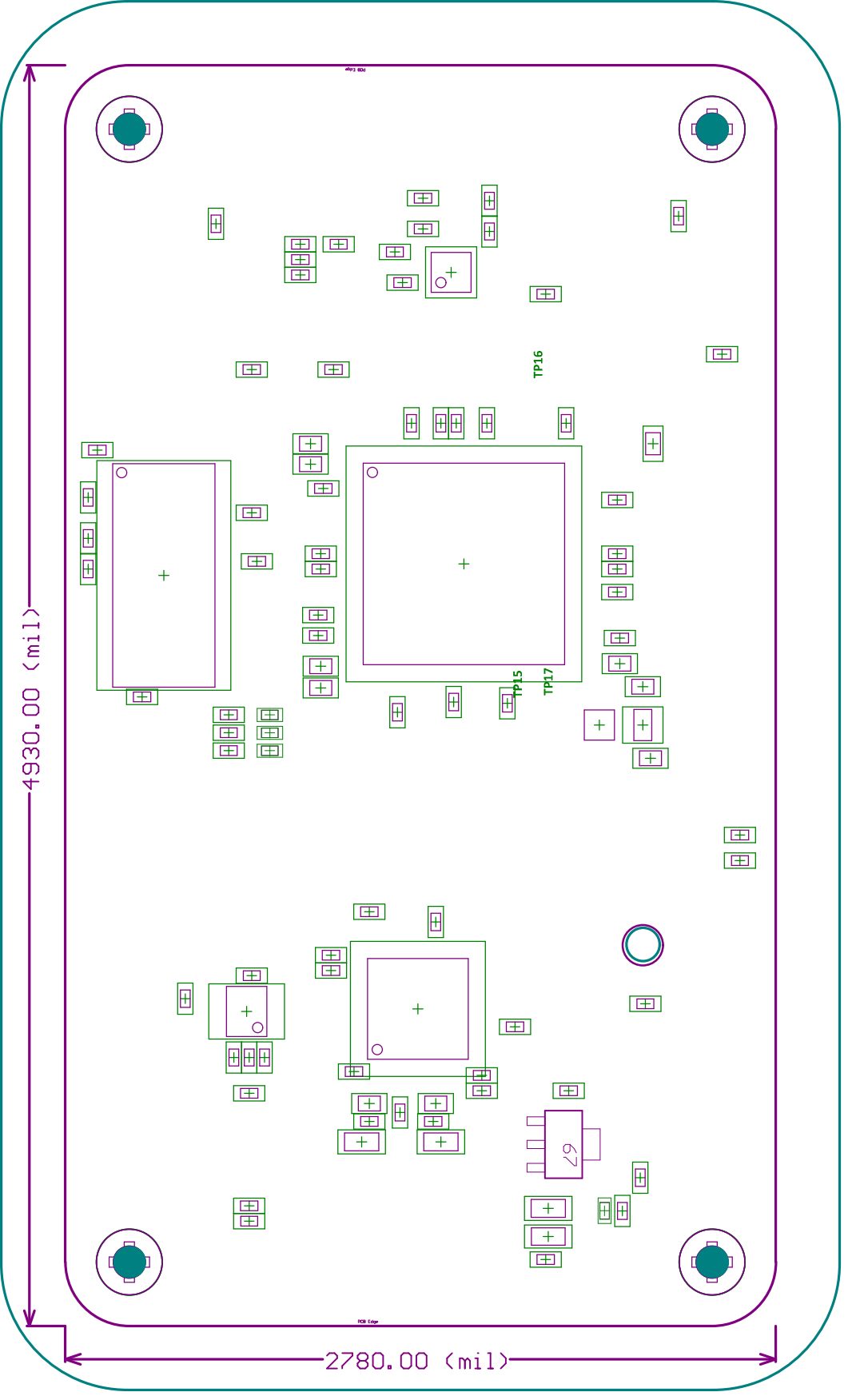
Mech2 (Acrylic)





Mechanical 1
Mech2 (Acrylic) Keepout
Mechanical 5
Mechanical 10
Mechanical 11
Mechanical 13
Mechanical 14
Mechanical 15
Mechanical 16

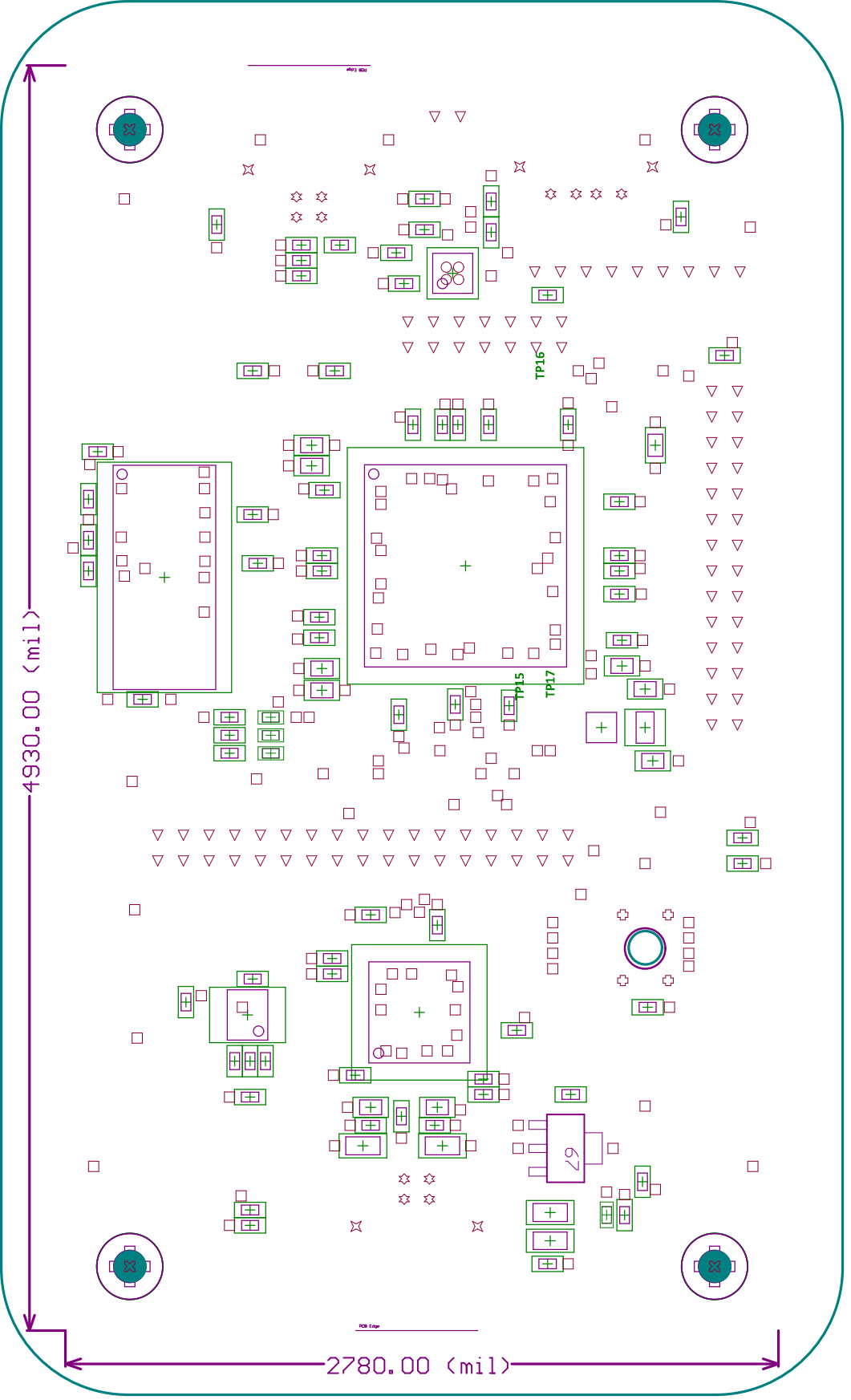
Size legend:
1 sq in

Layer Stack Up Detail for: ov_ftdi.PcbDoc

Layer Name	Gerber Document	Copper Thickness	Dielectric Height	Dielectric Material	Dielectric Constant	Dielectric Type
Top Solder Mask	(.GTS)		0.4mils	Solder Resist	3.50	
Top Layer	(.GTL)	1 oz	8 mils	FR-4	4.80	Core
Internal Plane 1	(.GP1)	1 oz	40 mils	FR-4	4.80	PrePreg
Internal Plane 2	(.GP2)	1 oz	8 mils	FR-4	4.80	Core
Bottom Layer	(.GBL)	1 oz				
Bottom Solder Mask	(.GBS)		0.4mils	Solder Resist	3.50	

Notes: unless otherwise specified

1. Silkscreen both sides with non-conductive, RoHS compliant ink not allowed on component pads or vias (color = WHITE)
2. Material: RoHS-compliant FR4, 1 oz copper on all layers
3. Solder mask: RoHS-compliant SMOBC, type LPI (color = RED)
4. Finish: ENIG
5. All hole sizes are after plating
6. Vendor may use tear drops to improve annular rings as long as DRC rules are followed
7. All finished pads to be 100% electrically tested



Mechanical 1
Mech2 (Acrylic)
Mechanical 5 Drill Drawing

Mechanical 11
Mechanical 13
Mechanical 14
Mechanical 15
Mechanical 16

Size legend:
1 sq in

Symbol	Hit Count	Tool Size	Plated	Hole Type
○	4	12.992mil (0.33mm)	PTH	Round
□	198	18mil (0.457mm)	PTH	Round
▽	87	35.433mil (0.9mm)	PTH	Round
✡	12	36.221mil (0.92mm)	PTH	Round
✣	4	39.37mil (1mm)	PTH	Round
⌧	6	90.551mil (2.3mm)	PTH	Round
⊠	4	125.984mil (3.2mm)	PTH	Round
	315 Total			

Drill Drawing.